51-channel analyzer for spectrum sampling. The SADISTOLOG - an analog level to digital converter

Liljencrants, J.

journal: STL-QPSR
volume: 3
number: 1
year: 1962
pages: 003-005

http://www.speech.kth.se/qpsr
B. 51-CHANNEL ANALYZER FOR SPECTRUM SAMPLING

The SADISTOLOG - an analog level to digital converter

General description

As part of the project outlined in STL, QPSR 1/1960 a unit named the SADISTOLOG has been developed to handle the rectified and smoothed outputs of the different analysis filters.

On the arrival of an order the unit takes a sample of the signal from the filter, then converts it to a digital measure which is stored in a counting register. The conversion is carried out on a logarithmic basis. Thus the content of the register is a binary number corresponding to the input level.

The spectrometer contains 51 analysis channels each of which is equipped with one SADISTOLOG. All the SADISTOLOGs are provided with reset and clock pulses, reference voltage, and power from a common equipment.

When the conversion is finished in all channels the registers are consecutively switched to the output of the analyzer, one at a time, with the aid of a set of ring counters and gates. The primary gate system is located within the SADISTOLOGs so that each will present the content of its register only on the occurrence of a readout pulse. The outputs of the SADISTOLOGs are connected in parallel in groups of ten. Each group is the by means of a secondary gate connected to the analyzer output. Channels 1 - 10 make the first group, 11 - 20 the second, and so on. Channels 1, 11, 21, ..., 51 are gated from the first stage in a ten stage ring counter, channels 2, 12, ..., 52 (of which the last one is "empty") from the second stage of the same counter etc. The secondary gates are governed by a six stage ring counter which will advance one step each time the ten stage counter has completed one cycle. Thus the scanning switch system has 60 positions of which the last nine are "empty" or may be used for special purposes.

Operation of the SADISTOLOG (Fig. I-2)

When no conversion is actually taking place a regulated reference voltage \( U_o = +50 \) V is fed to a parallel RC network through a diode thus keeping a certain constant charge in the capacitor. Before
Fig. 1-2. Circuit diagram of the SADISTOLOG. Numbers indicate terminals of circuit blocks. Transformer T: 2 x 20 turns on Philips pot core P 11/7, FXC 3H1.
the conversion the registers are reset to zero by a 10 μs pulse from
the clock pulse generator. On the trailing edge of this pulse the re-
ference voltage is switched off and the conversion starts. The feeder
diode is back biased and the RC combination will discharge giving a
voltage
\[ U = U_o e^{-t/RC} \] (1)

This exponential voltage is compared to the input signal
with a comparator similar to a multiam. The exponential voltage is fed
to the cathode of a comparator diode through the secondary of a pulse
transformer. This diode makes the series arm in a voltage divider.
The shunt arm of the divider is a resistor with its lower end connected
to the low impedance output of the signal source. When the exponential
voltage has fallen to a potential in the vicinity of that of the signal
the differential resistance of the comparator diode is rapidly diminish-
ing.

A closed circuit is formed by the voltage divider, a two
stage transistor amplifier, and a pulse transformer. When we have re-
ached a certain point of the diode characteristic the loop gain of the
circuit exceeds unity and regeneration takes place. Provided that the
regeneration starts at the time \( t_1 \) when the signal voltage \( U_1 \) and the
exponential voltage are equal we get the relation
\[ t_1 = -RC \cdot \log\left(\frac{U_1}{U_0}\right) \] (2)

At the start of the conversion a train of 127 clock pulses
is fed at an even rate to a seven stage scale-of-two counter through a
gate. At the regeneration point this clock gate is closed and the con-
version is completed. The number inscribed in the counter is then pro-
portional to \( t_1 \) and thus also to the level difference between \( U_1 \) and \( U_0 \).
The result of the conversion is stored in the counter till the next re-
set pulse appears. In the meantime it is possible to read the positions
of the counter stages any number of times.

The exact time of sampling is \( t_1 \) which means that the sam-
pling is not quite synchronous in all channels. By choice of a suffi-
ciently high clock frequency this time error can be hold within tolera-
bile limits.
Constructional details

The comparator diode is a silicon alloyed junction diode (Philips type 0A202). In the transition region a silicon diode has a relatively steep characteristic of differential resistance vs current. A certain point of this characteristic corresponds to unity loop gain in the comparator circuit. The voltage across the diode is then of the order of 0.5 V. In order to compensate for this voltage and its rather strong dependence of temperature a second diode of the same type is connected in series with the signal input. This compensation diode is forward biased with the current through a high resistance (4.7 Ohm) connected to a separate bias source (+85 V). The bias current is chosen to give approximately equal voltage drops across the comparator and compensation diodes at the regeneration point when the input signal is small. This compensation will give the comparator an accuracy of the order of 10 mV within the temperature range 20 - 50°C. At higher input levels the compensation is not so good when measured in terms of voltage, but in terms of level the error is entirely negligible. The clock frequency is 128 kc/s. Since the counter has seven stages it can count maximally $2^7 - 1 = 127$ pulses before returning to its zero position.

The time constant $RC$ is chosen to make the signal quantized in 0.5 dB steps ($RC = 136 \mu s$) and thus the total range will be 63.5 dB. The conversion time is always less than 1 ms and proportional to the level difference between reference and input voltages.

The counter stages and the binary controlling the clock gate are prefab bistable multivibrator circuit blocks (Philips type B8 920 00 FF1).

Preliminary tests have shown that the accuracy of the converter is within 0.5 dB over the entire operating range at stable environmental conditions. The upper limit of this range is $U_o$ which is chosen to 50 V according to the maximum output of the signal rectifiers. The useful dynamic range of the analysis channels are determined by these rectifiers rather than the converters.

Final tests regarding accuracy and stability will be made when the mechanical prototype which is under construction has been completed.

J. Liljencrants